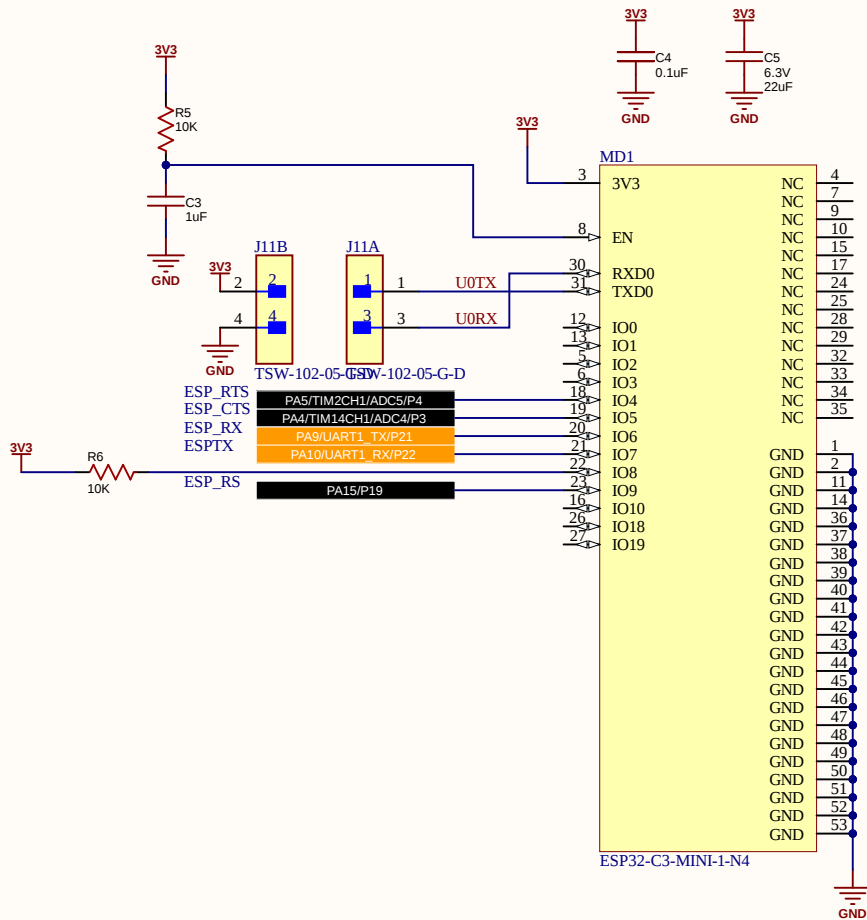




|                        |                                    |
|------------------------|------------------------------------|
| UART Pins <sup>1</sup> | TX: 7<br>RX: 6<br>CTS: 5<br>RTS: 4 |
|------------------------|------------------------------------|

| Boot Mode                             | GPIO2 <sup>2</sup> | GPIO8     | GPIO9 |
|---------------------------------------|--------------------|-----------|-------|
| SPI boot mode                         | 1                  | Any value | 1     |
| Joint download boot mode <sup>3</sup> | 1                  | 1         | 0     |

<sup>1</sup> **Bold** marks the default value and configuration.

<sup>2</sup> GPIO2 actually does not determine SPI Boot and Joint Download Boot mode, but it is recommended to pull this pin up due to glitches.

<sup>3</sup> Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot

GPIO2, GPIO8, and GPIO9 are strapping pins of the ESP32-C3FN4 chip. These pins are used to control several chip functions depending on binary voltage values applied to the pins during chip power-up or system reset. For description and application of the strapping pins, please refer to Section Strapping Pins in [ESP32-C3 Datasheet](#).



1

2

3

4

A

A

B

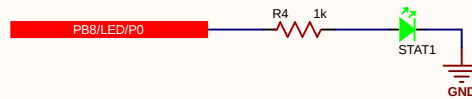
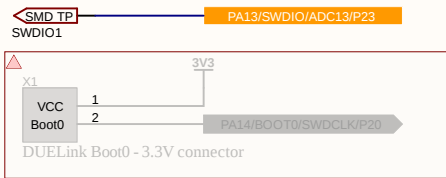
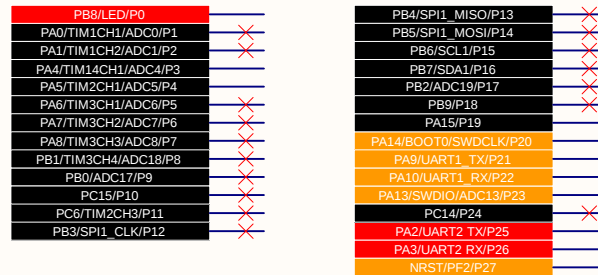
B

C

C

D

D

FID1  
Fiducial 40 MilFID2  
Fiducial 40 MilFID3  
Fiducial 40 MilFID4  
Fiducial 40 MilFID5  
Fiducial 40 MilFID6  
Fiducial 40 MilTitle: **MISC**Part #: **N/A**

Revision: A

Date: 2/24/2025

Sheet 3 of 5

501 E Whitcomb Avenue  
Madison Heights, MI 48071  
USA

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Software Features:

ADC: P1, P2, P3, P4, P5, P6, P7, P8, P9, P17

Pulse feedback: Can be any pin but hardware need 100pF + 1Mohm

HW PWM: P1, P2, P3, P4, P5, P6, P7, P8, P11

- \* P1, P2: TIM1
- \* P3: TIM14
- \* P4, P11: TIM2
- \* P5,6,7,8: TIM3

SW PWM: Any pin

SW UART: Pins 1 RX, 2 TX, 3 DBG

Wakeup Pins: P1, P3

Interrupts on: P1, P2, P3, P4, P5, P6, P7, P12, ....

Output compare: P2 (PA1)

Input capture: TBD

Neopixel: Any pin (blocking mode)

IR reciever: P1

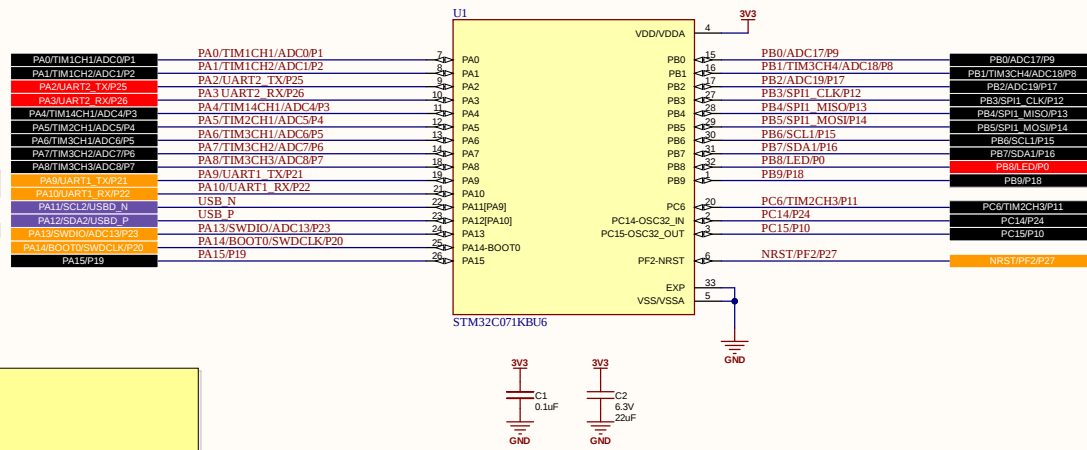
// PB8 - P0 -> LED  
// PA0 - P1 -> TIM1\_CH1 ADC0  
// PA1 - P2 -> TIM1\_CH2 ADC1  
// PA4 - P3 -> TIM14\_CH1 ADC4  
// PA5 - P4 -> TIM2\_CH1 ADC5  
// PA6 - P5 -> TIM3\_CH1 ADC6  
// PA7 - P6 -> TIM3\_CH2 ADC7  
// PA8 - P7 -> TIM3\_CH3 ADC8  
// PB1 - P8 -> TIM3\_CH4 ADC18  
// PB0 - P9 -> ADC17  
// PC15 - P10  
// PC6 - P11  
// PB3 - P12 -> SPI1\_CLK  
// PB4 - P13 -> SPI1\_MISO  
// PB5 - P14 -> SPI1\_MOSI  
// PB6 - P15 -> I2C1\_SCL  
// PB7 - P16 -> I2C1\_SDA  
  
// PB2 - P17 -> ADC19  
// PB9 - P18  
// PA15 - P19  
// PA14 - P20 -> SWCLK BOOT0  
  
// PA9 - P21 -> UART1 TX - Can be used when no Upstream  
// PA10 - P22 -> UART1 - Can be used when no Upstream  
// PA13 - P23 -> SWDIO ADC13  
// PF2 - P24 -> NRST - Reserved for emergency

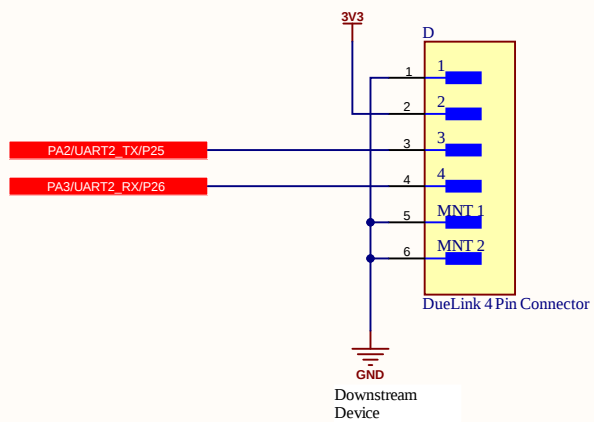
UART1 is available when not used in upstream

PA12 can be UART1\_CK

Sheet order priority:

- MCU.schDoc
- Downstream.schDoc
- Upstream.schDoc
- Misc.
- project\_name.schDoc





|                                  |                 |              |                                                           |                                                                                                                        |
|----------------------------------|-----------------|--------------|-----------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|
| Title: <i>DUELink Downstream</i> |                 |              | 501 E Whitcomb Avenue<br>Madison Heights, MI 48071<br>USA | <br>Where Hardware Meets Software |
| Part #: Downstream JST Connector |                 |              |                                                           |                                                                                                                        |
| Revision: A                      | Date: 2/24/2025 | Sheet 5 of 5 | ©2025 GHI Electronics, LLC.                               |                                                                                                                        |