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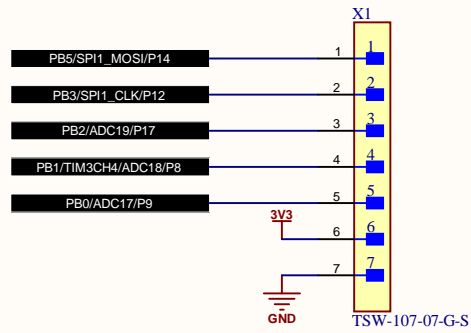
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Title: <i>VFD B8</i>				 Where Hardware Meets Software
Part #: GDL-DVFDB8-A				
Revision: A	Date: 4/4/2025	Sheet 1 of 5		
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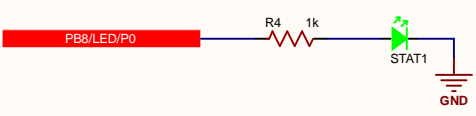
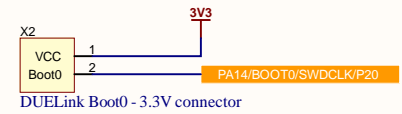
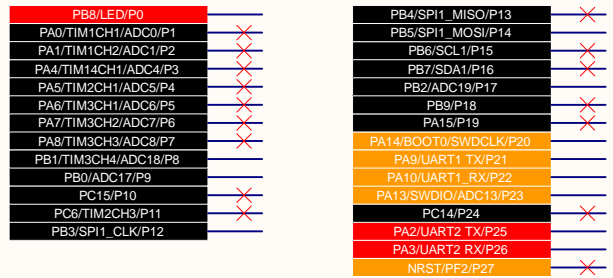
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Title: <i>Misc</i>		
Part #: GDL-DVFDB8-A		
Revision: A	Date: 4/4/2025	Sheet 2 of 5



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**Software Features:**

ADC: P1, P2, P3, P4, P5, P6, P7, P8, P9, P17

Pulse feedback: Can be any pin but hardware need 100pF+ 1Mohm

HW PWM: P1, P2, P3, P4, P5, P6, P7, P8, P11  
 \* P1, P2: TIM1  
 \* P3: TIM14  
 \* P4, P11: TIM2  
 \* P5, 6, 7, 8: TIM3

SW PWM: Any pin

SW UART: Pins 1 RX, 2 TX, 3 DBG

Wakeup Pins: P1, P3

Interrupts on: P1, P2, P3, P4, P5, P6, P7, P12, ....

Output compare: P2 (PA1)  
 Input capture: TBD

Neopixel: Any pin (blocking mode)

IR receiver: P1

```

// PB8 - P0 -> LED
// PA0 - P1 -> TIM1_CH1 ADC0
// PA1 - P2 -> TIM1_CH2 ADC1
// PA4 - P3 -> TIM14_CH1 ADC4
// PA5 - P4 -> TIM2_CH1 ADC5
// PA6 - P5 -> TIM3_CH1 ADC6
// PA7 - P6 -> TIM3_CH2 ADC7
// PA8 - P7 -> TIM3_CH3 ADC8
// PB1 - P8 -> TIM3_CH4 ADC18
// PB0 - P9 -> ADC17
// PC15 - P10
// PC6 - P11
// PB3 - P12 -> SPI1_CLK
// PB4 - P13 -> SPI1_MISO
// PB5 - P14 -> SPI1_MOSI
// PB6 - P15 -> I2C1_SCL
// PB7 - P16 -> I2C1_SDA

// PB2 - P17 -> ADC19
// PB9 - P18
// PA15 - P19
// PA14 - P20 -> SWCLK BOOT0

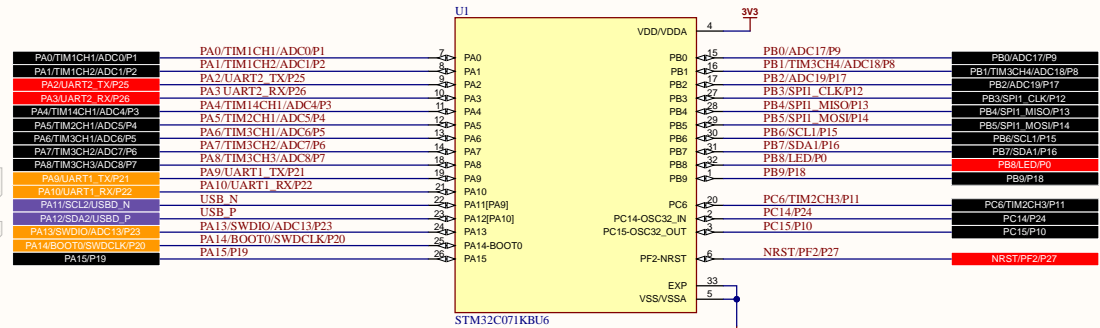
// PA9 - P21 -> UART1 TX - Can be used when no Upstream
// PA10 - P22 -> UART1 - Can be used when no Upstream
// PA13 - P23 -> SWDIO ADC13
// PF2 - P24 -> NRST - Reserved for emergency
  
```

UART1 is available when not used in upstream

PA12 can be UART1\_CK

**Sheet order priority:**

- MCU.schDoc
- Downstream.schDoc
- Upstream.schDoc
- Misc.
- project\_name.schDoc



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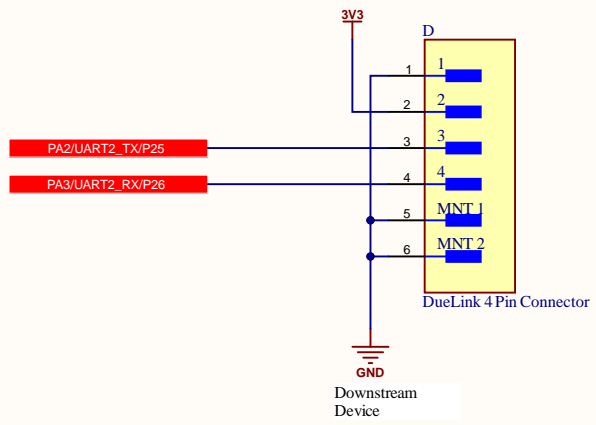
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Title: <i>DUELink Downstream</i>				
Part #: Downstream JST Connector				
Revision: v14	Date: 4/4/2025	Sheet 4 of 5	©2025 GHI Electronics, LLC - Michigan, USA	

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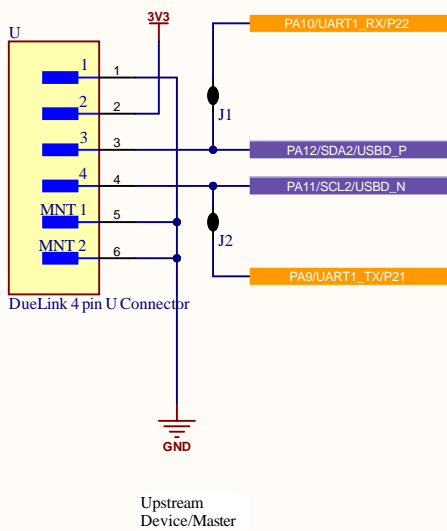
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Title: <i>DUELink Upstream</i>				
Part #: Upstream JST Connector				
Revision: v14	Date: 4/4/2025	Sheet 5 of 5	©2025 GHI Electronics, LLC - Michigan, USA	

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